

Preliminary Amendment

Applicant: Jong Chan

Serial No.: Unknown (Parent Application Serial No.: 09/085,204)

Filed: Herewith (Parent Application Filing Date: May 27, 1998)

Docket No.: 10980422-3

Title: **MEMORY CONTROLLER SUPPORTING REDUNDANT SYNCHRONOUS MEMORIES**

providing a plurality of control units, each control unit having a capability to control the transfer of data between the data processor and the data unit, each control unit having a memory device and signal paths coupled to the memory device, the signal paths enabling access to the associated memory device;

selecting one of the control units as a master control unit to control the transfer of data between the data processor and the data unit;

designating a second one of the control units as a slave control unit;

transferring the data between the data processor and the data unit by employing the memory device in the master control unit; and

synchronizing the memory device in the master control unit with the memory device in the slave control unit, the synchronizing including:

generating, in the master control unit, values for the signal paths associated with the master memory device to transfer data to the master memory device;

transferring a subset of the generated signal paths to the signal paths associated with the slave memory device; and

allowing the generated signals to perform the data transfer to the master memory device and the slave memory device.

38. The method of claim 37, wherein the generating step further comprises:

generating, in the master control unit, values for the signal paths associated with the slave memory device that enables access to the slave memory device.

39. The method of claim 37, further comprising:

associating an address and control signal path with each memory device that enables access to the corresponding memory device;

the generating step further comprising:

producing values for the address and control signal paths associated with the master memory device; and

the transferring step further comprising:

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transmitting the address and control signal paths associated with the master memory device to the address and control signal paths associated with the slave memory device.

40. The method of claim 39, further comprising:
 - associating with the master memory device a first control signal that controls access to the slave memory device;
 - associating with each memory device a second control signal that controls access to the corresponding memory device;
 - the generating step further comprising:
 - producing values for the first control signal and the second control signal associated with the master memory device; and
 - the transferring step further comprising:
 - transmitting the first control signal associated with the master memory device to the second control signal associated with the slave memory device.
41. The method of claim 39, further comprising:
 - associating with each control unit a data signal path; and
 - the transferring step further comprising:
 - receiving data values for the data signal path associated with the master memory device; and
 - transmitting the received data values to the data signal path associated with the slave memory device.
42. The method of claim 37, further comprising:
 - associating with the signal paths associated with each memory device a control mechanism that enables a transfer of values from a first signal path to a second signal path; and
 - enabling the control mechanism associated with the master memory device and the control mechanism associated with the slave memory device to transfer values between the master signal paths and the slave signal paths.

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43. The method of 42, further comprising:
disabling the control mechanism associated with a memory device to inhibit a transfer
and receipt of signal paths values.

44. The method of claim 37, further comprising:
suspending the master control unit from controlling the data transfer between the data
processor and the data unit;
enabling the slave control unit to control the transfer of data between the data
processor and the data unit; and
transferring the data between the data processor and the data unit by employing the
memory device in the slave control unit.

45. The method of claim 44, wherein the suspending step further comprises:
determining that the master control unit has experienced an operational failure.

46. The method of claim 45, wherein the determining step further comprises:
receiving an indication that the memory device in the master control unit has failed.

47. The method of claim 37, further comprising:
disabling the master control unit from accessing the slave memory device; and
suspending operation of the slave control unit.

48. The method of claim 37, wherein the disabling step further comprises:
determining that the slave control unit has experienced an operational failure.